ASSEMBLY OF 3D MICROELECTRONIC BLOCKS BY FOLDING

by
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Abstract

Integrated circuits are present in every electronic and computational device, and as such, efficient use of space is of major importance. Conventional technology relies on miniaturizing and connecting 2D circuits, but face heating problems and a lower limit restricting the minimum feature size. Although there are a couple of different methods for fabricating three dimensional circuits, they require a considerable amount of manual labor, are serial in nature and result in rather large structures. In this thesis, a new assembly method is presented that combines photolithography, electroplating and self-folding techniques to create micron scale polymeric cubes with circuitry and a microchip on its surface. This process takes advantage of the sequential layers of photolithography and electrodeposition to pattern circuitry on the outside of the planar nets. The folding process produces 3D cubes that minimize the footprint of the circuit. Self-folding is a fabrication technique that forms metallic or polymeric 3D polyhedral shapes from planar precursor nets by harnessing surface forces to drive the folding process. Compared to other methods of forming circuits, this method is highly parallel, minimizes the amount of manual input required and is defect tolerant by nature.

Additional applications of these polymer cubes were investigated such as patterning the circuitry on the inside of the cube, to insulate the circuit from the outside environment, and self-assembling the cubic units into a larger ordered computational device with increased processing power. Furthermore, these assemblies will not be plagued by heating issues like traditional computers, and will be able to more efficiently use the available space. Using these methods, progress toward creating a truly 3D

computer that mimics the design, power and connectivity of the human brain can be made.

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Chapter 1: Existing Methods of Integrated Circuits Design

Introduction

The continued downsizing of two dimensional integrated circuits and Complementary metal–oxide–semiconductor (CMOS) in the computing age has revolutionized nearly every facet of our lives by continuously decreasing the size of computers and handheld smart devices, while also increasing the computational power available. Presented in 1965, Moore's Law predicted that the number of transistors on an integrated circuit will double every two years for the at least the next ten years [1]. Since then Moore's Law has continued to hold, with the doubling time varying between 18 months and three years, due to new technologies [2]. Technologies such as copper interconnects, the prevalence of semiconducting materials and advanced nanofabrication techniques allow an increase of transistor density due to the miniaturizing of transistor size.

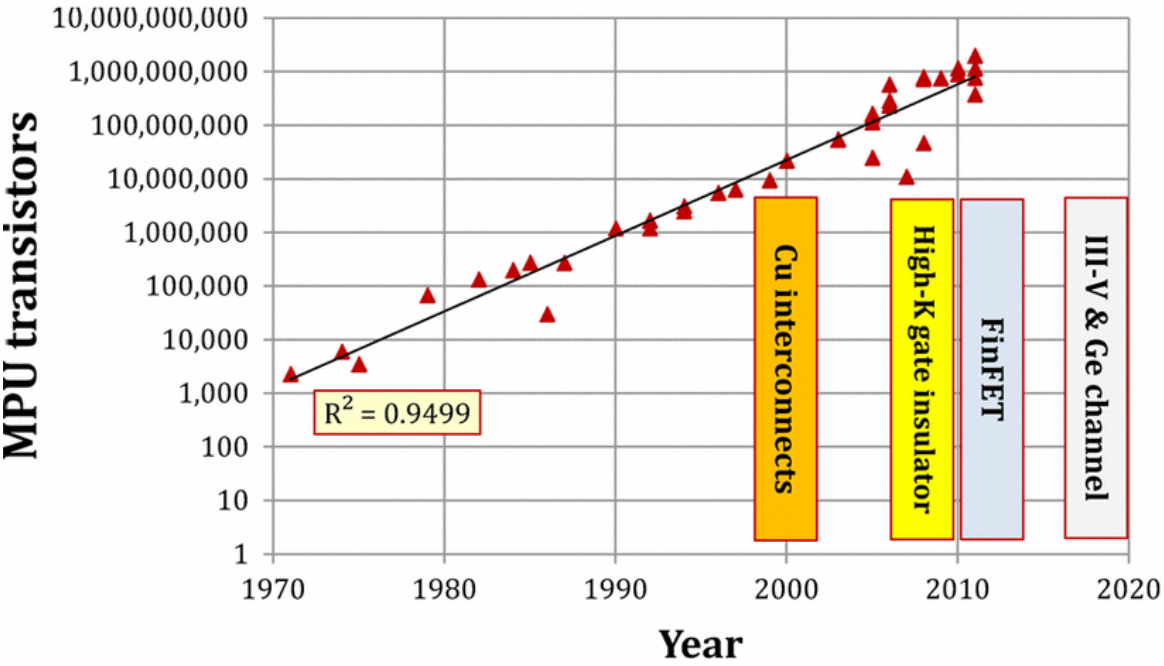

Figure 1: Projection of Moore's Law with Enabling Technologies. **A** plot showing data in agreement with Moore's Law proving the steady increase of transistors since 1970. Reproduced from reference [2], © 2012, with permission from IEEE.

Transistors have come a long way since the 1970s, when the minimum feature size was as large as 10 microns, to current transistors with a minimum feature size of 28 nm [3]. Figure 2 indicates that in the last 40 years there has been a four order of magnitude increase in device density.

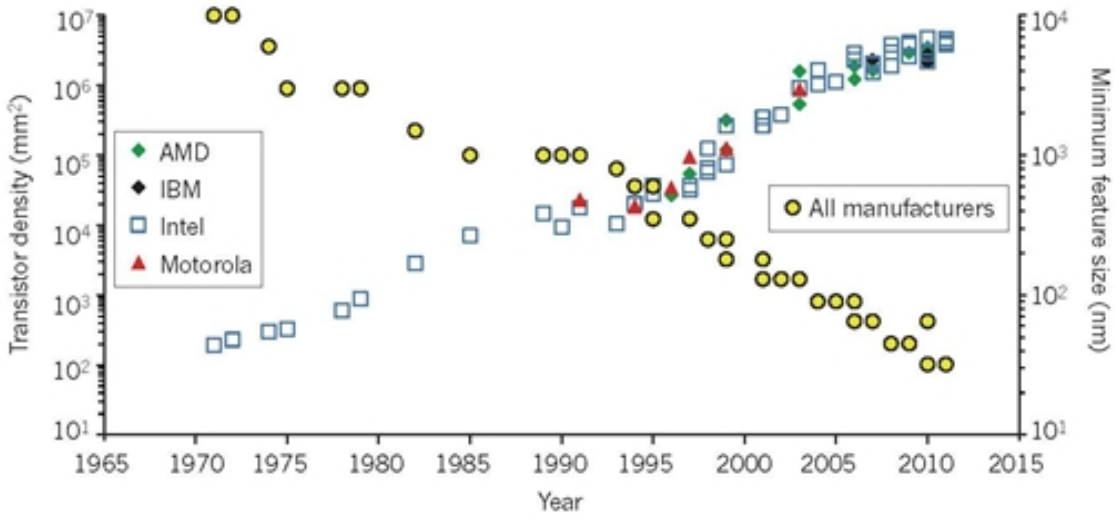

Figure 2: Double Line Graph of the Transistor Density and Minimum Feature Size Since 1970. A comparison of four different microchip manufacturer's progress at decreasing the minimum feature size of transistors, leading to an increasing transistor density in the past 40 years. Reprinted with permission from Macmillan Publishers Ltd: Nature. reference [3] © 2011.

Owning to the increasing transistor density, more transistors can be manufactured on a single wafer leading to decreased manufacturing costs. Another interesting effect of smaller and more efficient transistors is a decrease in total power consumption.

Despite documents from The International Technology Roadmap for Semiconductors that predict the growth of transistor density to slow towards the end of 2013 [4]. New technologies such as the multi-gate transistor should allow the trend of Moore's Law to continue until at least 2020 [5]. Nevertheless, there will come a time where Moore's Law will hit a wall due to a physical limit on the size of transistors. Fabricating transistors below 40 nm presents not only technological challenges, but also problems with heat dissipation [6]. When in a certain state, the power consumption from the power source is negligible. Nearly all of the power consumption occurs when a

transition takes place in the transistor state. After the transition takes place the transistor dissipates the excess power as heat, with the dissipation related to, among other factors, the geometry.

Even if Moore's Law continues to hold, microprocessors cannot hope to approach the power of a human brain. The human brain is capable of processing an enormous amount of sensory and cognitive information [7]. The neurons in the brain have an innate ability to organize themselves and automatically make connections with its neighbors. This gives human brains the ability to actively learn, reroute information around dead neurons and continue to make new connections throughout the neurons' life. The brain's more than 86 billion neurons, each with about 10,000 connections [8] indicates very efficient and dense three-dimensional packing. Higher density due to three-dimensional packing leads to high number of interconnects that enables the brain to transfer sensory information extremely fast. Despite the large number of neurons in the brain, the brain can still effectively dissipate heat due to spacing between each other that allows the body to pump fluids around the neurons to regulate their temperature and prevent the brain from overheating. The human brain provides an extraordinary template to model next generation integrated circuitry.

Chapter 2: Planar Circuits

The simplest arrangement of microchips for use in common computational devices are in a planar configuration. In a planar conformation, each one of the computing chips is arranged in a single, flat 2D layer [9]. This single layer design allows for horizontal connections between microchips to increase the total computing power available to the device [10]. The most efficient form of planar computing involves connecting the microchips on a single circuit board that allows each microchip in the array to interact with up to four near neighbors on the same plane.

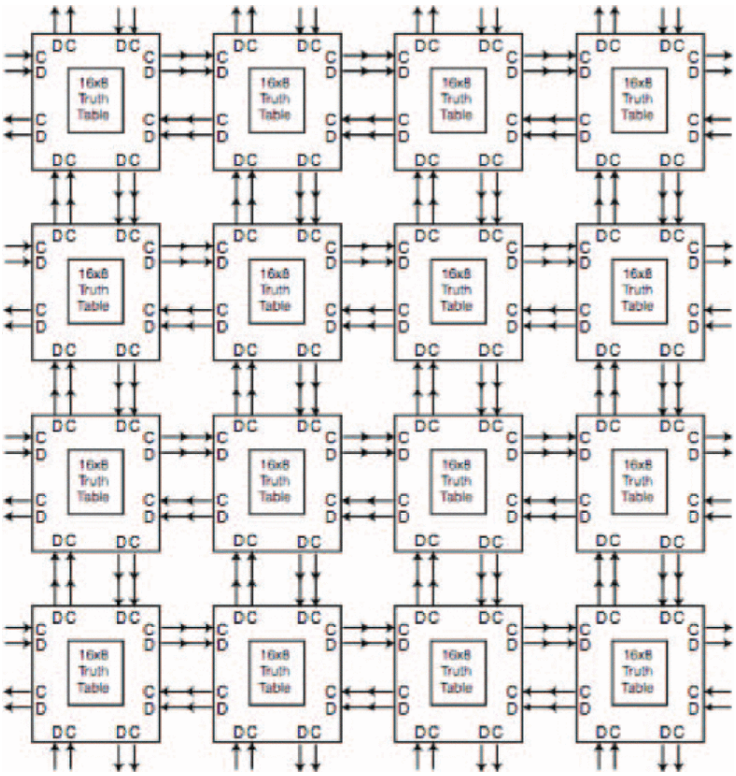

Figure 3: Planar Array Logic Circuits. 16 logic gates arranged in a single plane, each making connections with up to four near neighbors. Reproduced from reference [11], © 2013, reproduced with permission from IEEE.

The main advantage of this arrangement lies in the defect tolerant nature of this array. Since each chip can make connections with up to four other chips next to it, should one of the chips on the board fails the software can reroute the information around the defective chip to avoid a complete failure of the computation capabilities. The downside to the planar arrangement is that the number of chips, which dictate the computational power of the device, directly depends on the surface area available on the board [12].

In an effort to maximize and more efficiently utilize the space available in computational devices, developers have looked to ways to pack microchips in three-dimensional space. Since the chips are inherently two dimensional, with the ports connecting to wires linking chips together located on the underside of the chip, this limits the packing options. Methods other than the planar configuration involve wafer stacking, monolithic packing and die-to-die bonding.

Chapter 2.1: Wafer Stacking

Wafer stacking is a quasi-three dimensional, or 2.5 dimensional, arrangement used in devices such as commercially available computers that builds up on the planar configuration by taking advantage of the ability to vertically connect, or stack, the chips [13]. The most efficient packing occurs when the microchips are arranged on circuit boards in a planar configuration, and then connected to an identical layer situated either above and/or below that layer. To connect the different layers to one another, to link computing power and also power supply lines, an appropriate set of wires can run vertically up and down between the layers of the circuit board or the chips layers can be fabricated so that they physically interconnect with each other [14].

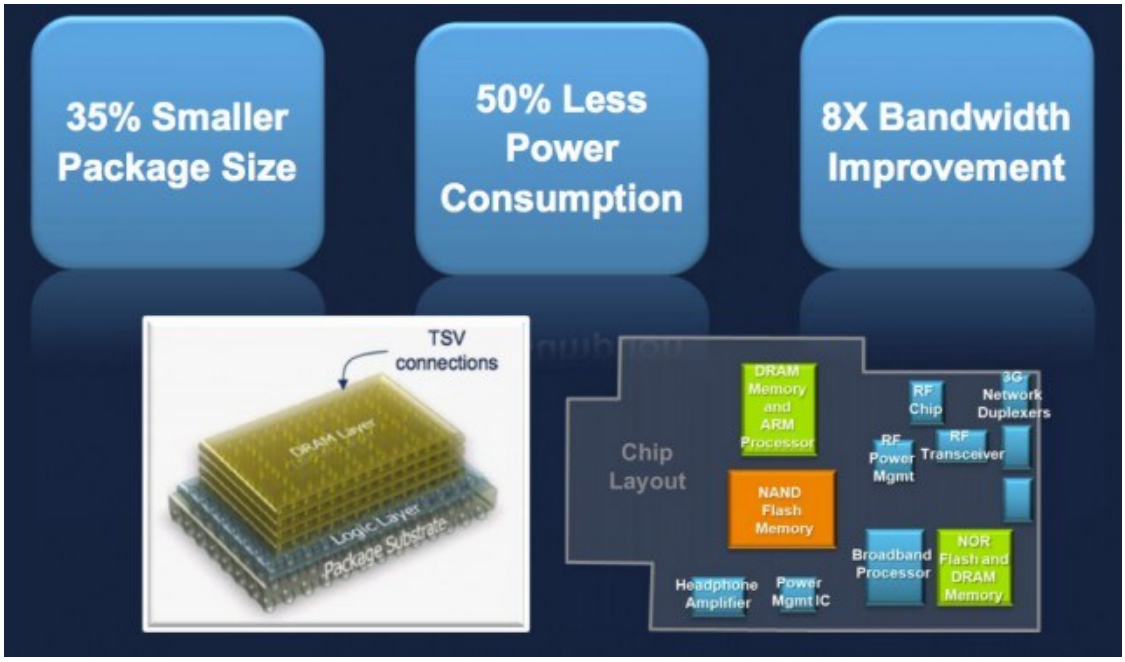

Figure 4: Wafer Stacking in Traditional Computers. Wafer stacking makes better use of the vertical direction and has benefits of smaller packing sizes and decreased power consumption. Reproduced from reference [15].

The main advantage of stacking lies in the ability to pack more parts into a smaller area by using free space that otherwise would be wasted. However, this approach is not truly three-dimensional because the chips are still only packed in two dimensions. While the stacked layers are macroscopically three dimensional, there is still wasted space between the layers. In addition, since the layers are arranged in series with shorter wires, the power requirement for the total stack is much less than if each layer were to be supplied its own power source [16]. Unfortunately, stacking does come with some downsides, namely that the close proximity and geometry of the packing does not allow for much heat dissipation or defect tolerance [17]. With the layers so closely packed, conventional techniques such as heat sinks cannot adequately direct the heat away necessitating a secondary cooling source such as continuously running fan or sophisticated liquid cooling system. These can lead to increased power consumption and

cost of the system. Without these systems the user runs the risk of melting and fusing the components together, which would ruin the device. As far as defect tolerance, since the layers are usually physically connected, the failure of even one of the middle layers can result in a catastrophic failure as neither the information nor power supply may no longer flow to the subsequent layer. In an effort to alleviate some of these faults, an insulator material is often placed between conductive layers to separate the different layers of circuits and prevent them from shorting out [18]. Another concern in the micro scale involves correctly aligning the layers on top of each other so that they can function properly [19][20].

Chapter 2.2: Wafer-on-Wafer Bonding

The last form of three-dimensional arrangement involves directly bonding the chips to each other in a process often referred to as 'die-on-die bonding' or 'die stacking'. Die bonding involves connecting two or more microchips with another material, often in a vertical orientation as to maximize the transistor density [21]. The material linking the layer is traditionally a dense metal that offers high conductivity between the wafers on opposite sides. This direct method of connection eliminates the need for wires, instead opting for a material that offers a high-speed data connection designed to minimize both the latency of signal transition and power usage [22].

The wafers to be bonded together are required to have the connecting ports facing both facing the connecting layer to allow for successful connection. With traditional components like RAM (Random Access Memory) chips in household computers only having one connecting face, limits the number of traditional wafers that can be bound to

two per connecting layer. In order to increase the number of bound chips one would need to uniquely design for the wafers or microchips involved so that they could accept connections on both faces in order to sandwich them between additional connecting layers as shown in Figure 5 [23].

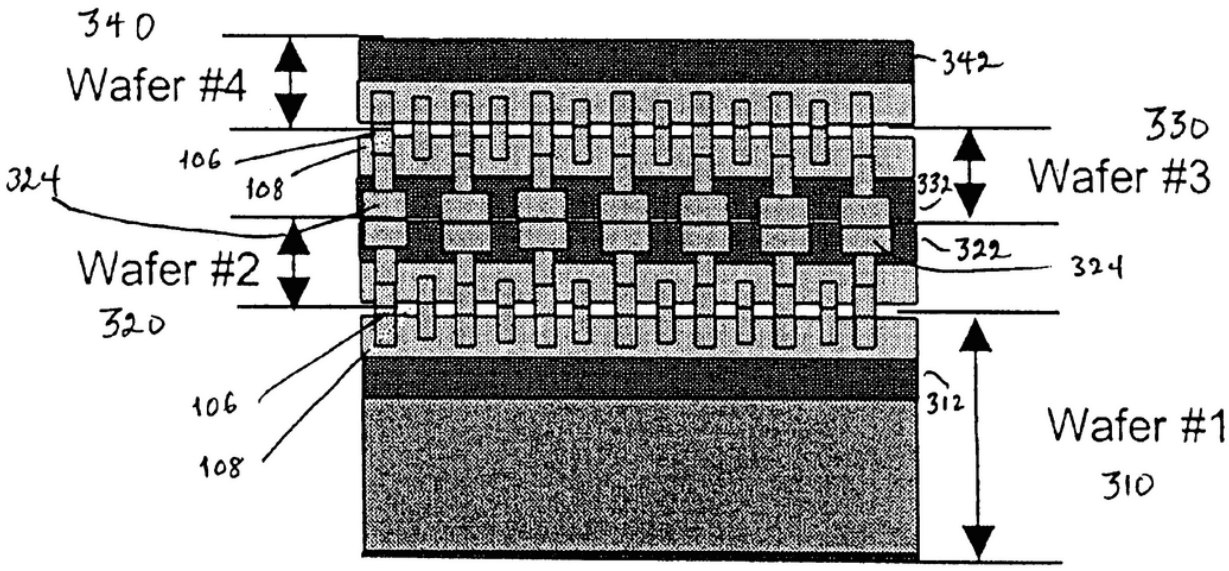

Figure 5: Graphic of Wafer-on-Wafer Bonding. Four wafers are perfectly aligned on top of each other model for wafer-on-wafer bonding. Each layer is bounded with a dielectric material enabling connections to share power and data inputs. Reproduced from reference [23], © 2005.

As previously mentioned, most of the difficultly preventing the wide spread use of wafer-on-wafer bonding approach involves difficulties in the micro-scale fabrication involved in patterning both sides of the layers such that the wafer can accept connection on both faces [24]. Additionally, such close packing and the inclusion of conductive metal layers allows for a buildup of heat, without the ability to adequately dissipate it [25].

Chapter 2.3: Three Dimensional Electronic Circuits

The transition from two-dimensional circuitry into three dimensions started with wrapping the circuitry around a frame, usually in the shape of a cube [11][26][27]. By wrapping the circuitry around a three dimensional structure one is able to increase the available surface area of an integrated circuit while maintaining the same footprint area [28]. This will allow for a massive increase in computing power without dramatically increasing the size of the electronic device. The two popular methods for creating three-dimensional circuitry include affixing multiple layers of circuitry on the outside of a shape or by including them inside of a hollow frame to hold the shape together.

Chapter 2.3.1: Robotic Pebbles

The robotic pebble system designed by Gilpin et al is capable of forming smart, programmable three-dimensional computational devices [29]. The basis for the device is a premade three dimensional brass frame in the shape of a cube with a length of 12m per side. The module contains electronic components such as chips and power capacitors attached to the inside of a flexible circuit that is wrapped around the frame.

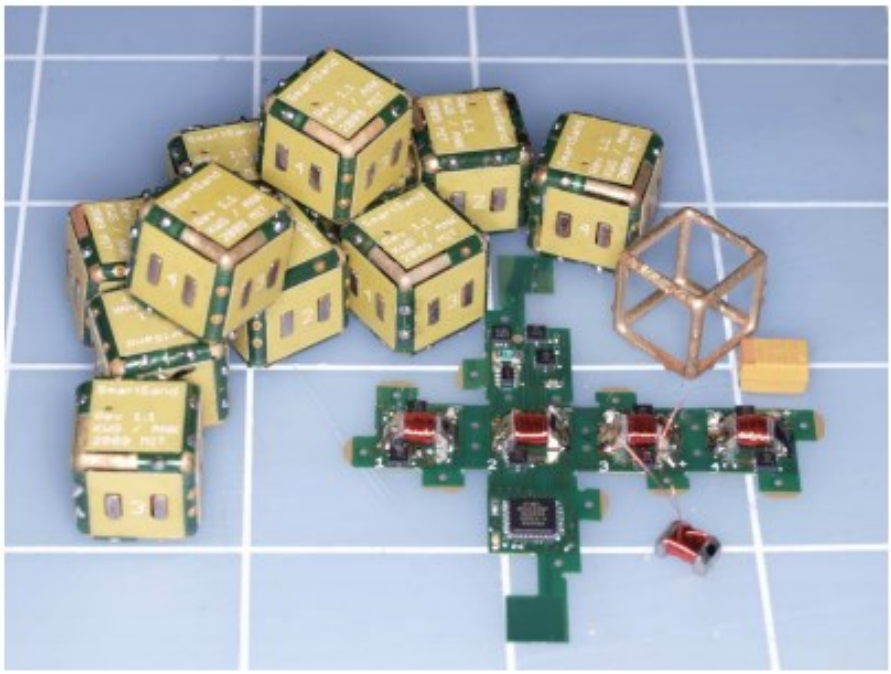

Figure 6: Robotic Pebbles. A collection of the programmable pebbles each with a side length of 12 mm along with the hollow brass frame and the flexible circuitry featuring electrical components. Reproduced from reference [29], © 2010, reproduced with permission from IEEE.

To facilitate self-assembly of blocks and communication of data and power an electopermanent (EP) magnet manually soldered to four faces of each cube. As a result of the four EP magnets, the pebbles can draw in and connect with up to four near neighbors in a crystalline structure without expending any energy. Application of an external magnetic field can also cause the structure to disassemble as well.

Each part of these pebbles must be manually put together before the device can function. Their relatively large size alleviates some of the difficulty in making the manual soldering connections between the flexible circuitry and electronic parts while also sporting a high yield of functional devices. If a system can take advantage concepts presented here, namely the intelligent use of space, programmable chips and self-

assembling properties, while also reducing the size and manual fabrication steps, then one could create a truly autonomous three-dimensional computational device.

Chapter 2.3.2: Cell Matrix Architecture and Electronic Blocks

The Cell Matrix Architecture is based on a system of smart polyhedral units, either cubes or octahedral, connected via a reconfigurable electronic fabric [11]. Each individual cell can modify its neighbor's truth table allowing for circuits that can self-regulate themselves. Fabricated three-dimensional integrated circuits into what are called 'E-blocks" have demonstrated the ability to transfer both data and power signals through surface patterned wires [30].

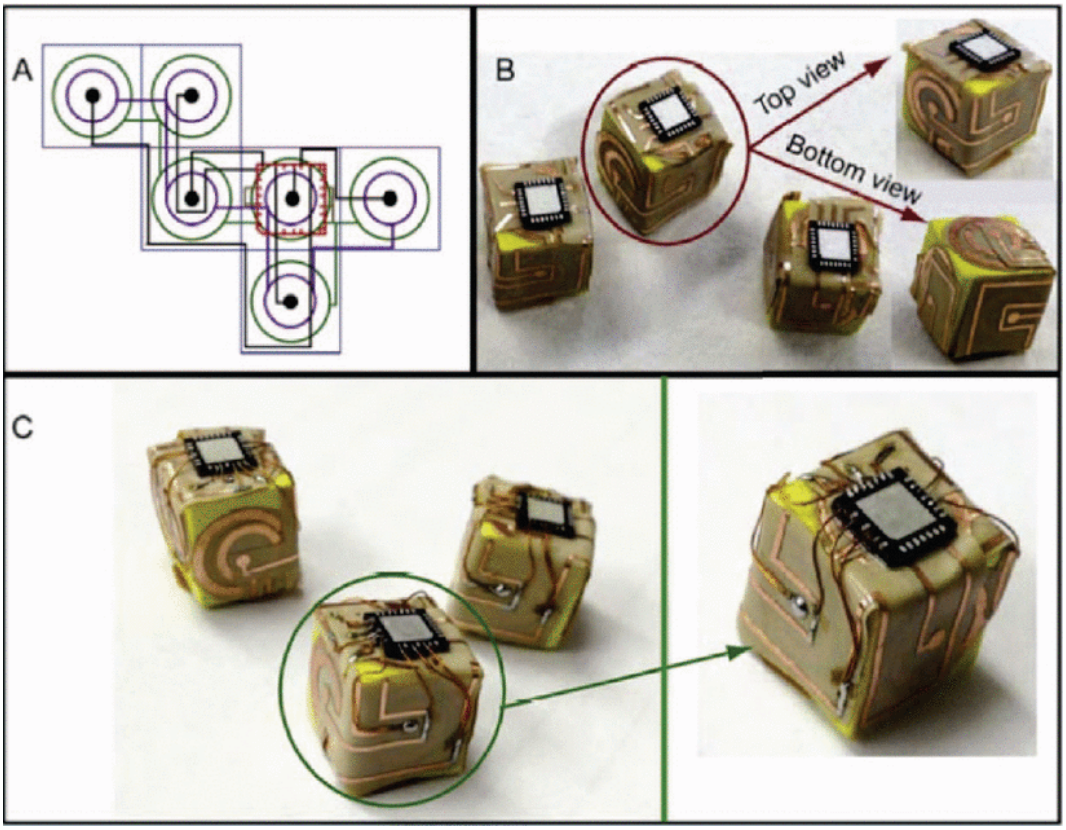

Figure 7: Functional Three-Dimensional Electronic Blocks. (a) Schematic of the different layers of circuitry with each one carrying a different signal; (b) top and bottom view of the E-blocks; (c) close up of the solder

connections enabling communication with the attached chip. Reproduced from reference [11], © 2013, reproduced with permission from IEEE.

These E-blocks are often solid shapes with the circuitry patterned on the surface through electroplating or manually cut out and glued to the faces of a cube. The base for these E-blocks can take nearly any shape and size provided that the process for patterning the circuits can adapt to the dimension and remain unbroken when folded around the corners of the faces. The two dimensional matrix can also be extended into a three dimension array by assembling the blocks adding an additional two near neighbors. This three dimensional cell matrix has the benefits of adaptive programming, enhanced fault tolerance due to the uniform units and only near neighbor interconnects [31] and ability to scale the size of both the units and matrix itself.

While these methods can produce fully functioning three-dimensional circuits and even computational devices, their fabrication is extremely time consuming and difficult. These E-blocks require three separate layers of circuitry, with each one carrying a different signal, cut out and glued on top of each other so that the different layers do not interact or short. In addition, the thin wire interconnects between adjacent E-blocks must be manually soldered to each other under a microscope. In each of these steps human error can greatly affect the yield of functional particles as even one broken wire can render the entire block useless.

Chapter 3: Surface Tension Driven Self-Folding

Self-folding is the process where the surface tension produced by reflowing hinges causes a two dimensional precursor 'net' to curve or fold into a three dimensional structure [32][33]. In order to dictate the three-dimensional shape that the structure will form one must first design a planar net that contains all of the pieces of the final structure. The planar net includes the panels that will make up the folded structure along with hinge gaps for the material that will generate the stress needed for folding. Photolithography is a popular choice for patterning the panels and hinges due to the high precision and relative ease of use. The hinge material is often a low melting point material, that when raised above its melting point, will reflow and ball up in an attempt to minimize its interfacial free energy. Each molecule in the hinge material is attracted with an equal amount of force from every direction; however, the molecules sitting at the liquid-air or liquid-surface interfaces do not have neighboring molecules to exert a force on them. As a result of the unbalanced forces, the near-by molecules generate an internal pressure that pulls the interface inwards contracting the bulk to form the shape with the smallest possible surface area [34]. This contraction generates a torque that pulls the panels and dives the folding process. Thus, self-folding is a method for producing three dimensional shapes, provided that a corresponding two dimensional net can be mapped out in the form of a mask in a computer aided design program [35]. In fact, the only limitation to the shape of the net and even the patterning appearing on the final structure depends on the ability to produce the appropriate net in the design program. Figure 8 shows some examples of different three-dimensional structures than can be fabricated using this self-folding technique.

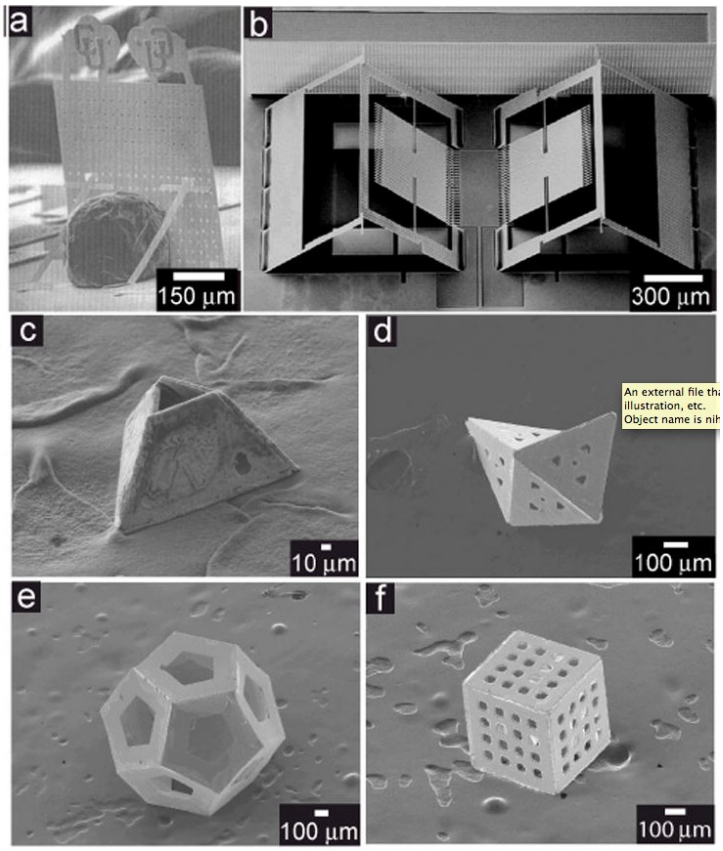

Figure 8: Examples of Surface Tension Driven Self-folded Three Dimensional Shapes. (a) Solder based self-folded plates with kickstands (b) interlocked reflectors fabricated via surface tension driven self-folding (c-f) solder based self-folding of truncated pyramids, boat shape octahedron and a porous cube. Reproduced from reference [36], © 2010, with permission from John Wiley and Sons.

In self-folding, the folding angle depends on both the type of hinge material and the amount of material present in the hinge gap. Figure 9 depicts a graph showing the dependence of folding angle based on the volume of tin-lead solder hinges, a very popular low melting point hinge material.

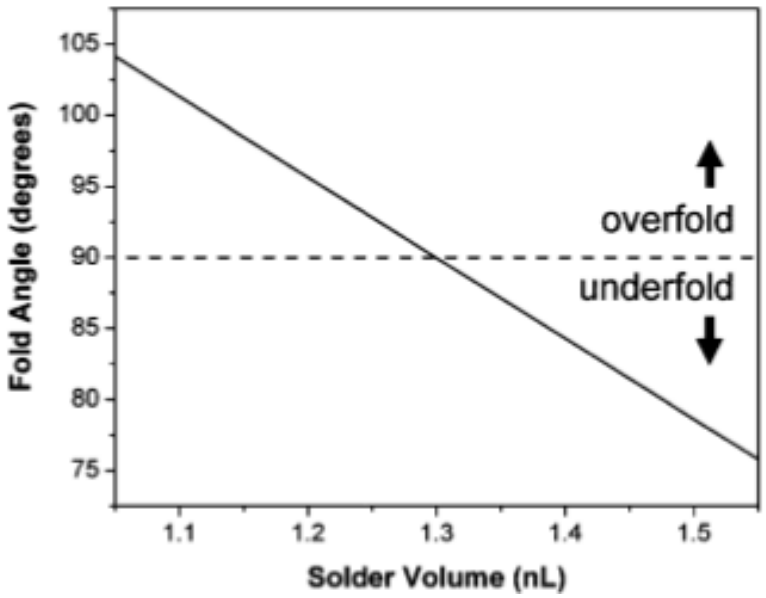

Figure 9: Finite Element Simulation for Dependence of Fold Angle on the Amount of Hinge Material. Finite Element Simulation on a 200 micron cube. The fold angle can be controlled by the volume of hinge material. Reprinted with permission from reference [37] © 2014, with permission from Springer.

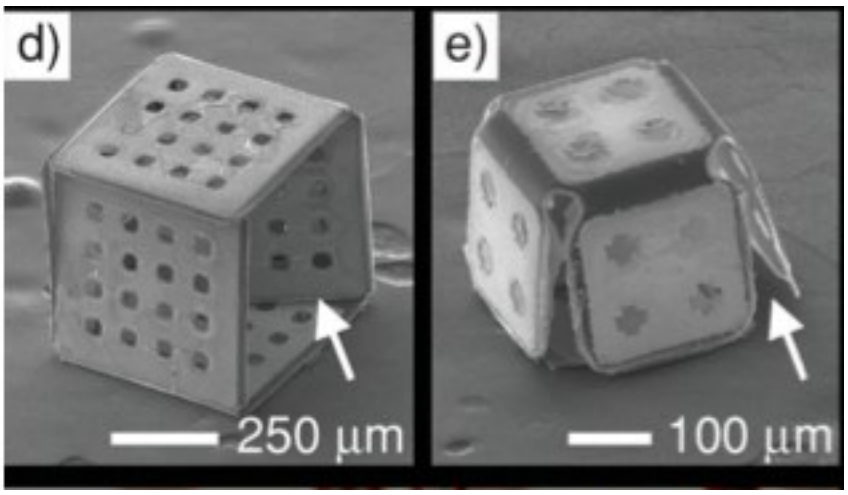

Figure 10: SEM Images of Cubes with Various Defects. **(**d) 500 micron cube with over folded hinge (e) 200 micron cube with under folded hinges less than 90°. Reproduced from reference [36], © 2010, with permission from John Wiley and Sons.

The hinges are not simply limited to generating the driving force for folding the panels, but can also be designed to seal the edges of connecting panels together to hold

the shape of the structure indefinitely. In the simple case of a three dimensional cube, the hinges placed between two panels will act as folding hinges, while those placed on the periphery of the cube's two dimensional net will act as locking hinges.

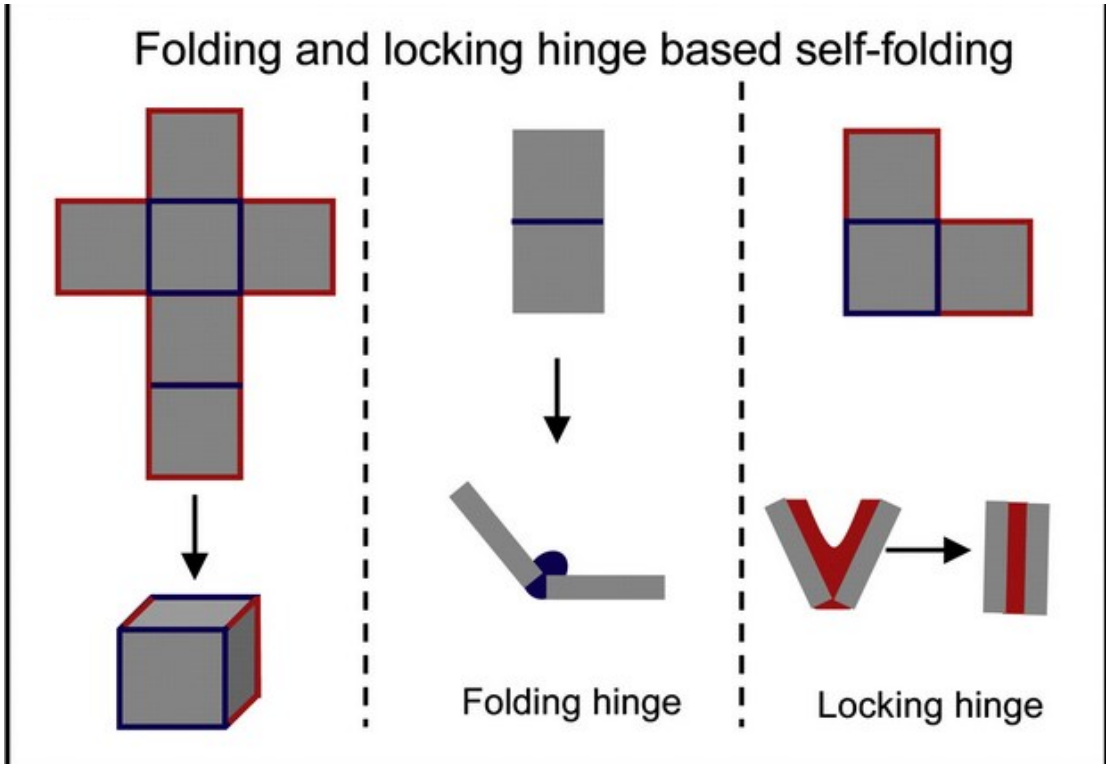

Figure 11: Schematic Showing the Different Types of Surface Tension Driven Self-Folding Hinges. The hinges in blue correspond to folding hinges responsible for generating the torque required to fold panels. The hinges in red correspond to the locking hinges that seal to keep the three-dimensional shape of the structure. Reproduced from reference [38], © 2012, with permission from Elsevier.

Since the principle behind surface tension driven self-folding is highly versatile, one can interchange the materials that make up the panels and even the hinges to yield a variety of three-dimensional geometries and of vastly different sizes. For example, the structures shown in Figure 8 are comprised of metallic panels linked by low melting point tin-lead solder; however it is also possible to pattern the panels using a photopatternable polymer such as SU-8 and use another polymer like polycaprolactone as the hinge material to produce cube shaped three dimensional structures with patterned faces [39].

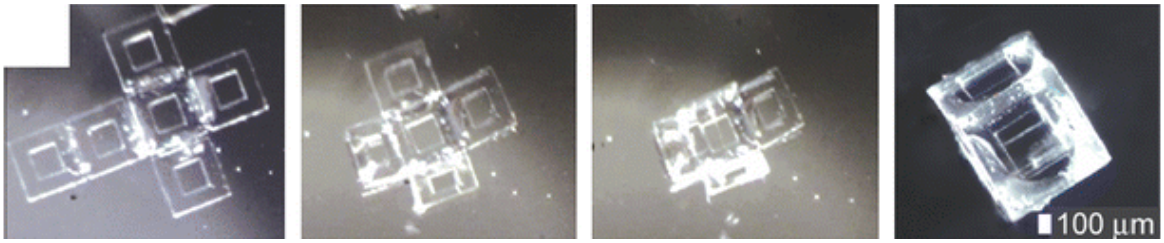

Figure 12: Self-Folding of a SU-8 Polymeric Container. A cube made of SU-8 panels with PCL hinges self-folding in 60° water. Reproduced from reference [39], © 2011, with permission from Springer.

Self-folding can be used to create a multitude of three-dimensional shapes with sizes ranging in scale from nanometers to millimeters. Furthermore, the process offers the advantages of being highly parallel, so they can be mass-produced, tetherless, and even biocompatible if fabricated with the appropriate materials. Owning to the ease of augmenting the fabrication process to produce nearly any three dimensional shape and surface pattern, the dependability of the tension driven self-folding phenomena, and the wide range of materials available one can tailor the use of these polyhedral to biological applications, cargo delivery or electronic circuits.

Chapter 4: Fabrication of Three Dimensional Electronic Circuits

Photolithography, an inherently two-dimensional fabrication technique, has been a staple in microfabrication processes ranging from chip making to patterning faces on self-folding polymeric containers [40] [38]. Fabricating complex structures using photolithography is a very common and relatively straightforward, provided that an appropriate mask design can be created. As mentioned in **Chapters 2-3**, the combination of photolithography and stress driven self-folding has enabled the creation of a variety of truly three-dimensional structures, with a variety of applications [41][42][43].

The sequential nature of photolithography permits the patterning of different layers of features on the structure. Conventional self-folding techniques, such as thin film stress based and surface tension, can be used to fold these two dimensional nets into three dimensional structures, but their surface patterns are often designed to demonstrate the flexibility to pattern nearly any shape [44], for biological [45] and polymeric [46] adhesion studies, or used for shape matching self-assembly purposes [47].

Polyhedral shapes, such as cubes, octahedrons and dodecahedrons, made ideal candidates to carry electrical circuitry because their regular and repeating units can compactly fit together to create larger order circuits. Three-dimensional circuits have traditionally been fabricated by hand and on the centimeter and millimeter size. Here we report a process that combines sequential photolithography and electroplating steps with self-folding methods enabling formation of functional cube shaped three-dimensional integrated circuits on the micron scale.

Instead of conventional metallic self-folding polyhedral, we use a polymer to form the basis of the cube to avoid electrical shorts that happen with metal on metal contact. The polymer panels necessitate the use of a polymeric hinge material because solder would have nothing to bond with. This is a parallel process, where the number of units simultaneously created only depends on the surface area of the wafer as compared to the size of the two dimensional net. Because circuit will lie on the outside of the cube, the structures need to be fabricated in a backwards way. In this process, compact two-dimensional cubic and a wire surface pattern nets and are created in a computer-aided design program. A photolithography step patterns the wells where the wires will sit on the surface of the folded structure. The next step involves patterning the panels for the cube with another photolithography step. After that, the polymeric hinges are manually added to the hinge gaps. The nets are then lifted off of the wafer by dissolving the sacrificial layer to release them. Finally, a microchip is attached to the net and placed in hot water to fold the structures to their final shape.

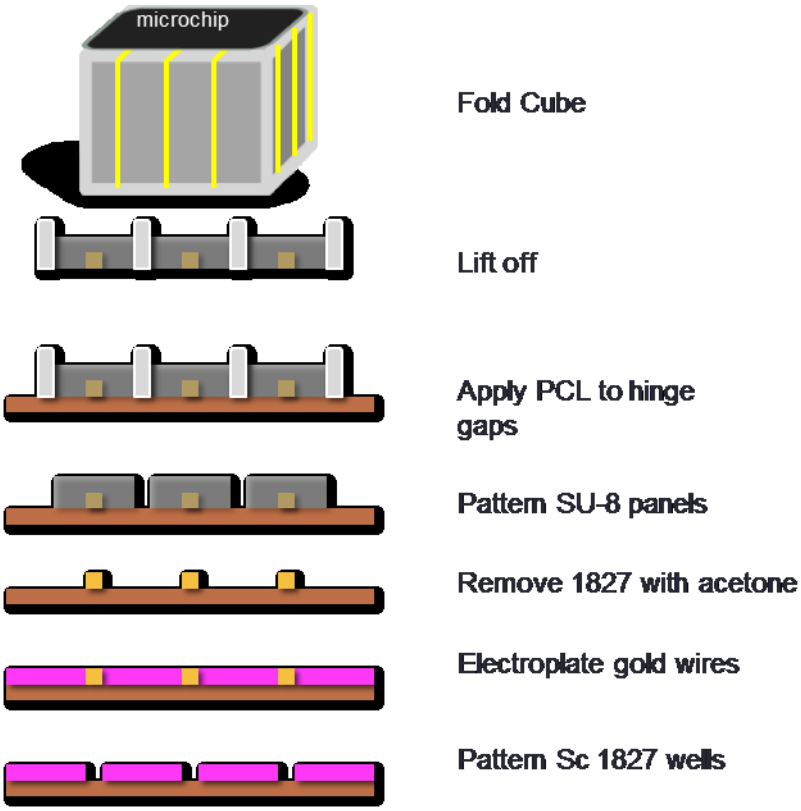

Figure 13: Fabrication Strategy for 3D Cubes with Wiring. The backwards fabrication process for creating a three dimensional cube with wires and a microchip on the surface.

Chapter 4.1: Fabrication of Non-patterned SU-8 Polymeric Cubes

Previous attempts at folding polymeric cubes chose to use SU-8 as their material, another polymer for the hinges and restrict the size to a few hundred microns [38]. Inspired by that success, we decided adopt much of their protocol for the fabrication of the cube, except to increase the size of our cubes to better suit more complex circuitry. To test the viability of self-folding to create larger cubes with a panel length of 500 microns, we chose prove the concepts first with non-patterned cubes then move on to adding the circuitry. We used Autodesk AutoCAD to draw both the cubic net and wire pattern and then printed the designs onto transparent sheets to form photo masks. The most compact

cubic net was chosen to maximize the yield of successfully folded cubes [48][49], with a hinge gap of 7.5%.

Starting with a silicon wafer, first a thin (30 nm) layer of chromium was thermally evaporated at 10^{-5} torr onto the wafer to enhance bonding of the copper sacrificial layer (150 nm) to the wafer. Next, Su-8 2025 polymer was spin coated onto the copper layer at 1,000 rpm to produce panels approximately 70 microns thick. Using the cubic net mask and an ultraviolet (UV) light source the exposed areas of SU-8 were selectively photocrosslinked with an energy of 160 $\frac{mJ}{cm\hat{}2}$. Developing in the SU-8 developer (1-Methoxy-2-propyl acetate) for five to ten minutes, or until a white residue no longer formed over the features, removed the uncrosslinked SU-8 to reveal the panels and hinge gaps.

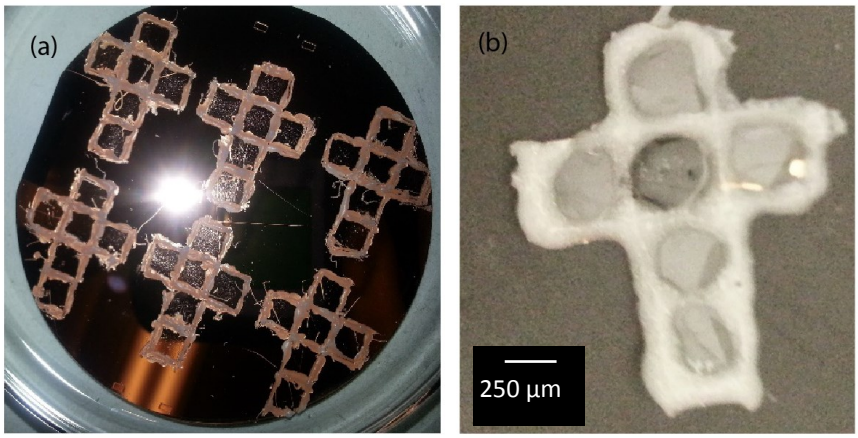

Figure 14: Cubic SU-8 Net with PCL Hinges. (a) Shows an entire wafer of nets on a wafer (b) a single unfoled structure after lift-off

Polycaprolactone (PCL) of 10,000 molecular weight (melting point approximately 60° C) was melted and manually applied via a syringe tip to the hinge gaps and periphery to create the folding and locking hinges in Figure 14. The entire wafer was then placed in APS-100 over night to dissolve the copper sacrificial layer and release the unfolded structures. Folding took place in water heated above 60° C.

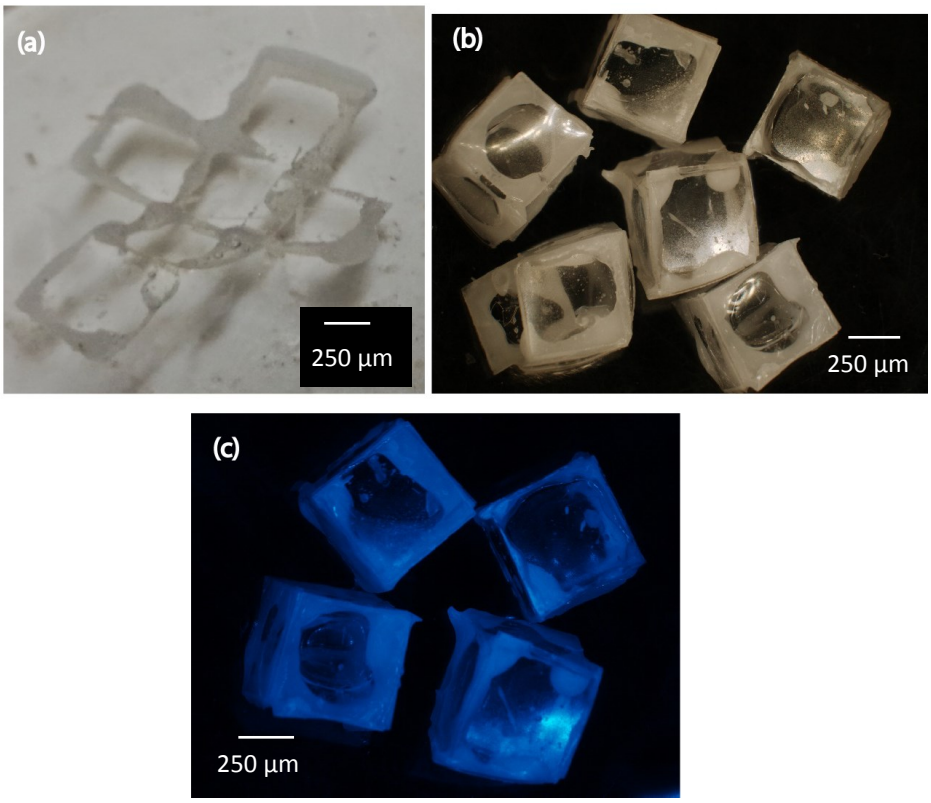

Figure 15: Images of Non-patterned SU-8 Cubes. (a) A cube in the process of self-folding (b) optical microscopy of folded cubes and (c) fluorescent image of folded cubes

Successful folding allowed us to proceed to the addition of circuitry on the cube faces.

Chapter 4.2: Cubes Surface Patterned Circuitry

The addition of wires required an additional step of photolithography and electroplating. Before photopatterning the panels, a layer of Microposit 1827 is spun onto the wafer at 3,000 rpm to produce a film 27 microns thick. UV exposure using the mask with the wire design and subsequent developing in MF 351 developer created wells to dictate where the wires will lie on the cube. Because the lift-off process would also remove wires made of copper, gold was chosen to form the wires. The wafer was immersed in a gold electroplating solution to plate out gold wires into the wells produced in the previous step to form the net shown in Figure 16.

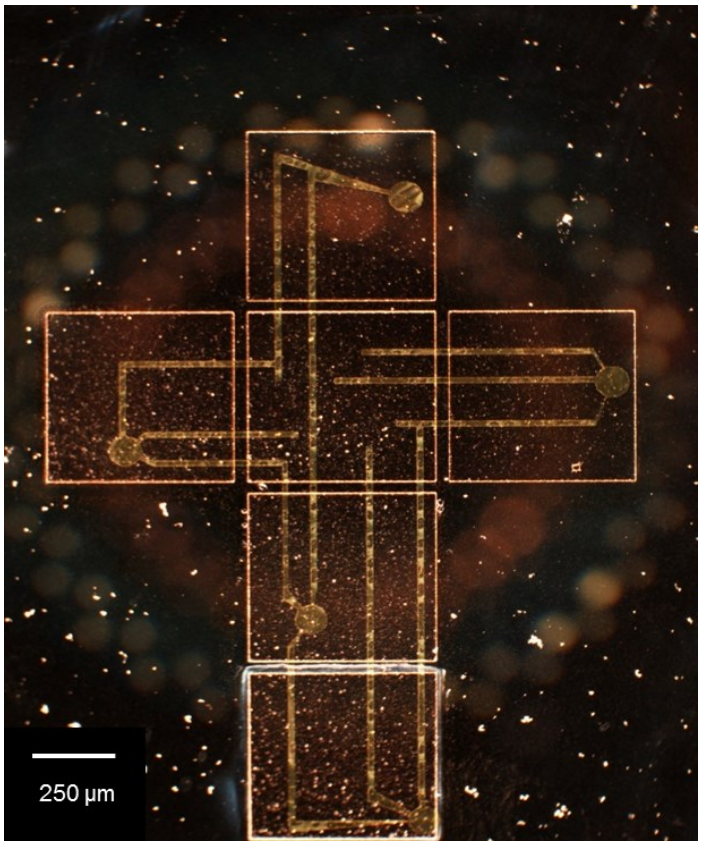

Figure 16: Optical Miscopy of 2D Net with Wires. Optical microscopy of SU-8 panels with underlying gold wires still attached to a wafer.

After forming the wires, removal of the remaining 1827 photoresist on the wafer is important so that thin film stresses do not arise between the 1827 and SU-8 that would impede proper folding. After forming the wires, photolithography, hinge patterning and folding procedures continue as before resulting in cubes with wires on the outside surface as seen in Figure 17.

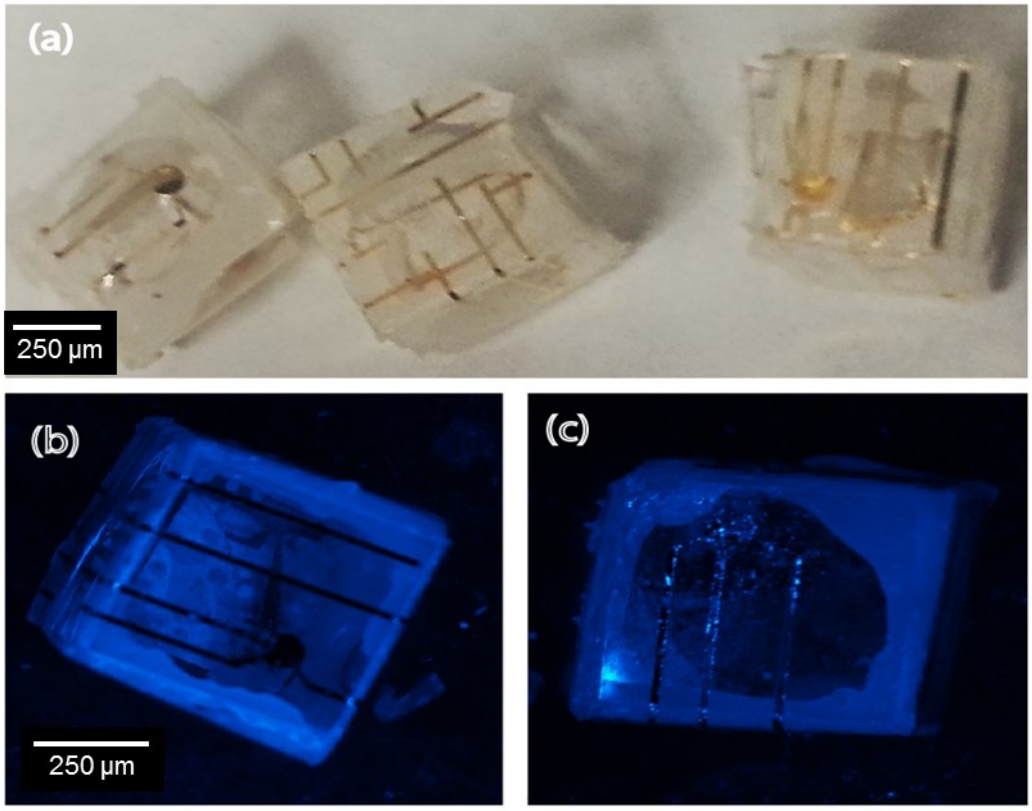

Figure 17: Images of Cubes with 3D Circuitry. (a) Optical microscopy of a three SU-8 cubes illustrating the different patterns of gold wiring. (b,c) Fluorescent microscopy of two different faces featuring gold wiring on the surface of a single cube.

Each face of the cube has different pattern of wires that are linked at a circle on the face. This maintains connectivity with each face and with any other cube connected adjacently.

Chapter 4.3: Addition of a Microchip

Due to the flexibility afforded by the self-assembly process, attaching a microchip to the cube to form an integrated circuit can occur at almost any step and location on the cube.

Chapter 4.3.1: Surface Attachment

To form cubes with a surface carrying the integrated circuit as in Figure 18, the cube can be affixed with an epoxy resin either before or after folding. If attaching the microchip pre-folding, the microchip should be attached to the backside of the center panel in the compact net as to not add extra weight to any of the moving panels that would prevent folding. After folding, the chip can be attached anywhere on the cube because the wires maintain connectivity throughout all faces.

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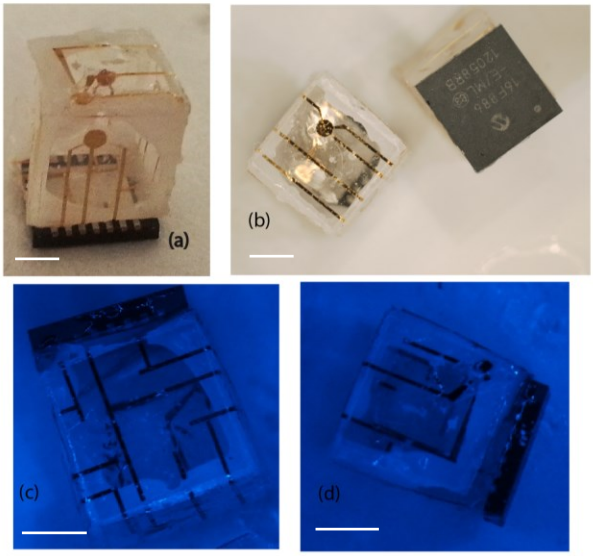

Figure 18: Three-dimensional integrated Circuits with Exterior Microchip. (a,b) Optical microscopy of SU-8 cubes with integrated circuitry seen with the microchip on the bottom and top, respectively. (c,d) Fluorescent microscopy of the microchip attached to the outside of the cube. All scale bars are 250 μm.

Chapter 4.3.2: Interior Attachment

The microchip can also be placed on the inside of the pre-folded net and have the cube fold around it, thus encapsulating the chip to protect it from the outside environment. This is of particular interest when placing the wiring on the inside of the folded cube. Placing the wires on the interior of the cube can be accomplished by first patterning the SU-8 hinges, then patterning the 1827 photoresist wells and thermally evaporating gold into the wells. Because the PCL hinges will seal and prevent the liquid from entering and shorting out the circuit, a liquid can be pumped around the cubes to facilitate cooling. Once again, locating the microchip in the center panel remains essential for proper folding of the cube. If placed on any other panel, the weight of the chip

disrupts the folding, as the PCL hinges cannot generate enough force to close the other panels around it.

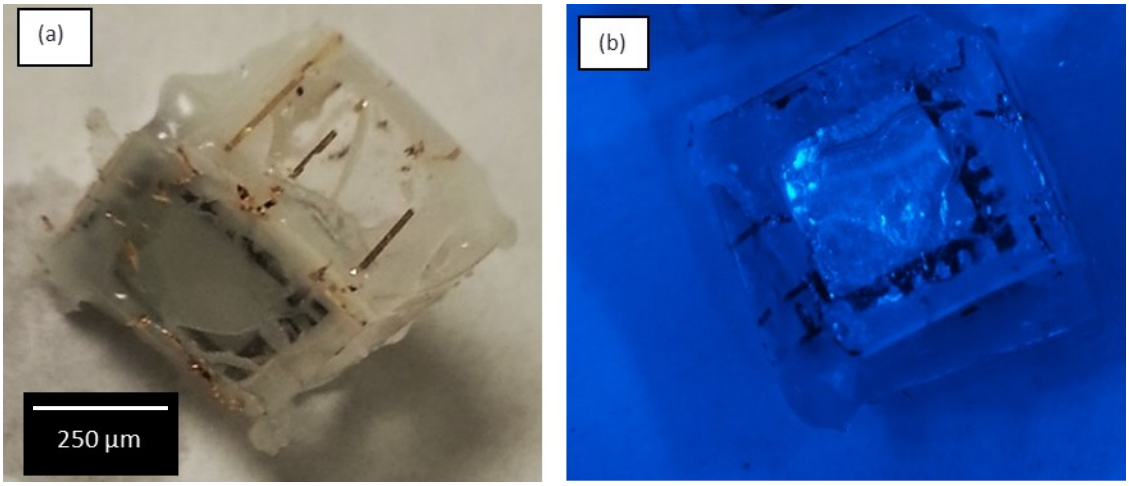

Figure 19: Three-dimensional integrated Circuits with Interior Microchip. (a) Optical microscopy of a cube with a gold wires and a microchip on the inside. (b) Fluorescent microscopy of the microchip inside a folded cube.

Chapter 4.4: Discussion of Results

This chapter illustrated two different methods for fabricating micron sized three-dimensional cube shaped integrated circuits. The combination of photolithography, electroplating and self-folding allows the parallel fabrication of numerous cubes per wafer without much manual effort. The all polymer cubes make for great electrical insulators to prevent the circuit from shorting. The identically shaped units are ideal building blocks to compose a self-assembling circuit. The processes are highly scalable as well, only limited by the size of the microchip. Furthermore, the three-dimensional nature and polymer composition are well suited to dissipating heat away from the circuit to both the interior and away from the cubes, potentially solving an important problem in computing.

The final yield for successful folding of lift-off cubes is estimated at between 25-33%. Reasons explaining the low yield, as well as explanations of the defects are discussed in **Chapter 5.**

Chapter 5: Defects and Mitigation

During the fabrication process many defects occurred along with quite a few challenges that necessitated solutions in order for this project to succeed.

Chapter 5.1: Optimization of Panel Material and Thickness

Choosing to fabricate the cubes out of a polymer instead of the traditional nickel metal raised the question of which type of polymer to use. 1827 could not be used because it was too thin and not robust enough. SU-8 was chosen for its photopatternability, ability to create straight high aspect ratio sidewalls for the panels, robust nature and a wide range of thicknesses.

Three SU-8 varieties were available including the 2015, 2025 and 2050 versions, with the last two digits indicating the thickness in microns when spun at 2,000 rpm for 1 minute. The 2015 variety was ruled out because it would not be thick enough to support the wires or weight of the microchip and would crack under the folding stress. The thick panels produced by the 2050 was plagued by long development times that lead to the panels ending up partially underdeveloped or cracking due to over developing in some regions. In addition, the panels seemed too heavy for the PCL to fold. At this speed the 2025 also suffered from chipped panels due to the small thickness.

To solve this problem the speed was reduced to 1,000 rpm. Once again 2015 spread too thinly to be a viable choice, while the 2050 version was extremely viscous, often leading to uneven spreading across the wafer. 2025 was able to produce a uniform coating across the wafer, develop in a timely manner and avoid cracked or chipped panels upon lift-off and folding.

Chapter 5.2: Folding Problems

A number of problems stood in the way of successful self-folding of the cubes. This section will detail them, starting with the most prevalent defects first.

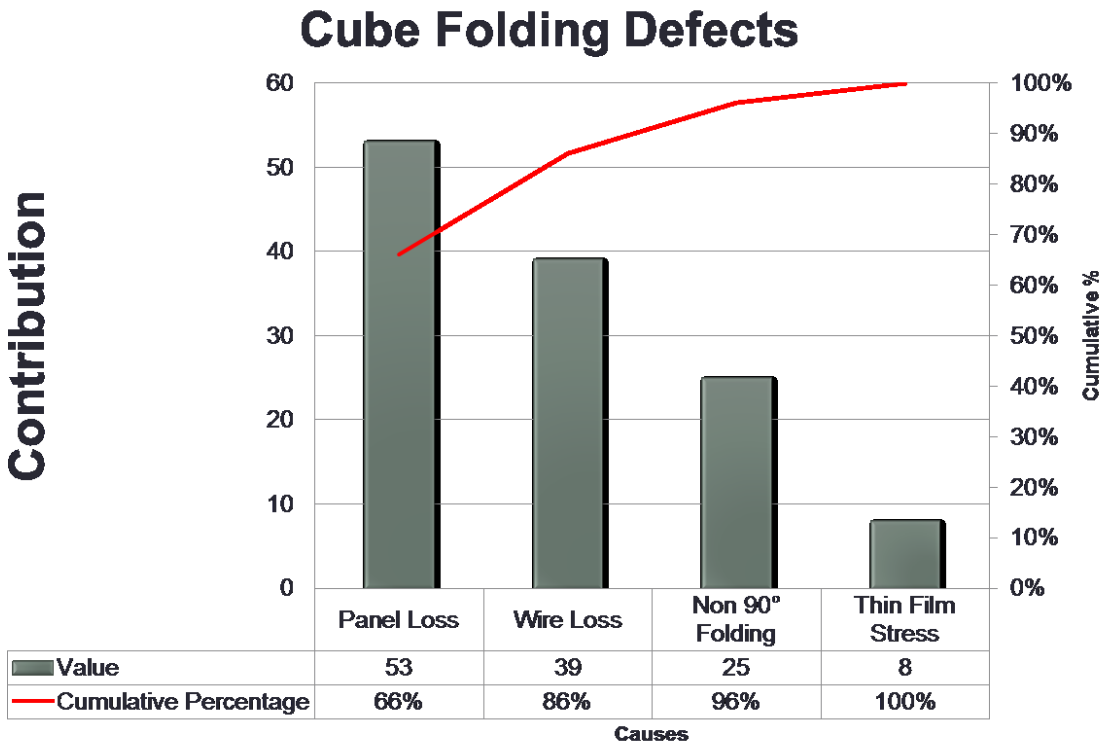

Figure 20: Pareto Defect Analysis. This Pareto chart details the contribution of each defect type experienced over 125 folding attempts.

Chapter 5.2.1: Loss of Panels

The single greatest contributor to the low yield of folding came from a loss of one or more of the panels during folding and lift-off. During folding, the PCL melts and reflows to minimize its surface area providing the driving force for folding. Often times when the PCL was in the process of melting and reflowing, but before folding could occur, one or more of the panels would become detached from the net as a result of

insufficient PCL to hold it in place. This usually occurred at the corners of the outermost hinges, resulting in half attached or completely detached panels, as shown in Figure 21.

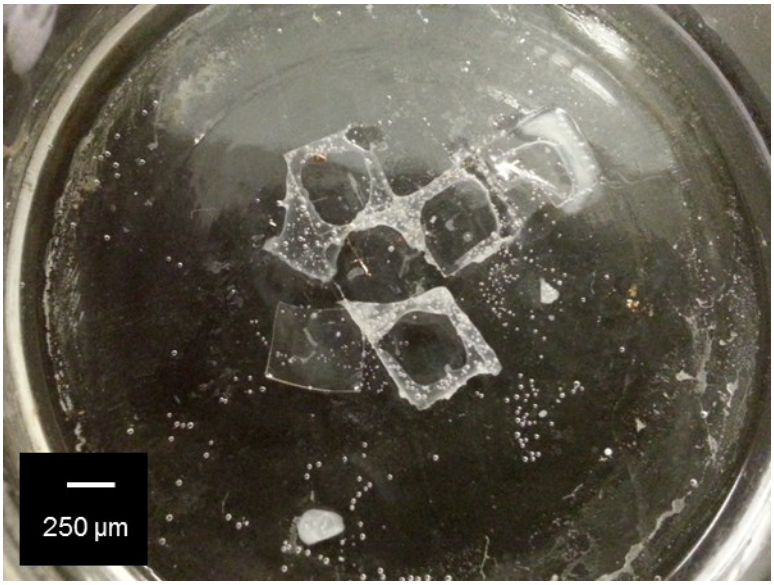

Figure 21: Detached SU-8 Panel. The lack of PCL in the center of hinge gap between the top and center panels leads to detached panels.

The first way to remedy this was to insure that the hinges were evenly coated with sufficient PCL to prevent a thin spot from detaching. The second involved reducing the hinge gap from the traditional 10% [44] to 7.5%. This reduced the loss of panels and also shortened the length that the PCL had to reflow and strengthened the folding force.

Although APS-100 is very good at etching away the copper sacrificial layer during lift-off, its efficacy and speed was greatly reduced by the presence of the PCL at the edges of the panels and the gold wires. The rate-limiting step in the lift-off process was the lateral diffusion of the APS-100 under the features, so every time it encountered something it could not etch it would have to look for gaps to seep between. Occasionally, the APS-100 would simply not be able to get underneath a panel to dissolve the copper and the panel would remain bound to the wafer. Prolonged exposure in APS-100 dried,

cracked and degraded the PCL hinges resulting in broken panels. The compromised hinges could no longer generate enough surface tension to fold the net.

Figure 22: Broken SU-8 Panels. Incomplete lift-off and prolonged exposure to the copper etchant result in broken panels.

Chapter 5.2.2: Loss of Wires

Sometimes the gold wiring would not remain bound to the cube and drift off into the solution. The most likely cause appeared to be incomplete bonding with the SU-8 panels. Most often happened during the lift-off process when some of the panels would partially lift-off, but the wires would remain on the panels. Other theories include excess agitation shaking them lose during transfer out of the APS-100 solution or interaction with the etchant.

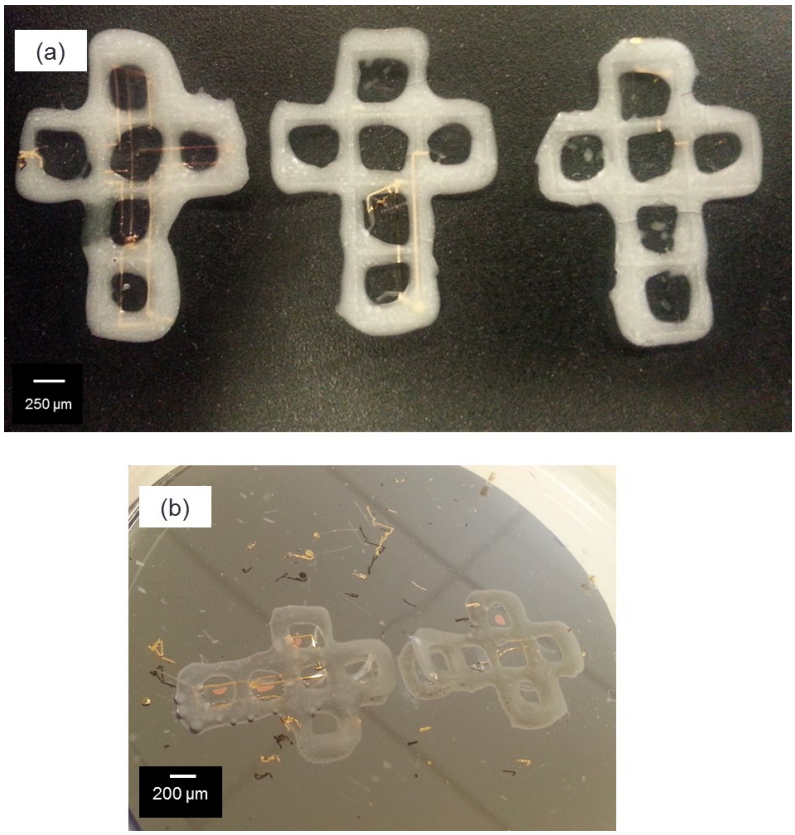

Figure 23: Loss of Wiring. (a) Varying degrees of wiring loss on cube nets from only one panel missing on the left to almost no visible wiring on the right most net. (b) Detached wires floating in copper etching solution during the lift-off process.

Chapter 5.2.3: Non-90° Folding

The next most serious problem involved either incomplete (under folding) or over folding. This issue mainly had to do with the amount of PCL on the hinges and the temperature of the water. Under folding tends to occur when force exerted by the reflowing action of the hinge material, as determined by the amount of PCL, could not support the weight of the panel. The obvious solution to this problem is to load a large amount of PCL into the hinge gap, however, adding too much PCL would cause it to ball up at the vertices and physically impede the edges from reaching 90° and sealing. This would lead to an under folded or open cube.

If the water were not hot enough to melt the PCL then no folding would take place, but if the water were too hot (over about 80° C) over folding would predominate.

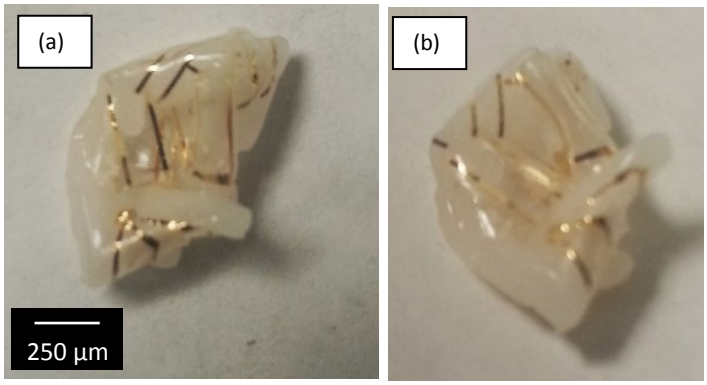

Figure 24: Over Folded Cubes. (a,b) When the water exceeses 100° C the structure over folds in a deformed way.

When heated too much the PCL would suffer two fates. If the water was only slightly too hot, the PCL would aggressively pull the panels together and deform the structure as in Figure 24. If the water exceeded 100° C the PCL would flow out of the hinge gaps and the panels would detach.

Chapter 5.2.4: Thin film stresses

Thin film stresses occur when different layers of materials, with different thermal coefficients or lattice mismatches, come into contact with each other [50]. The differences in material cause a stress that bend or otherwise deform the layers. The first attempt at using 1827 photoresist to pattern the tracks for the wires and then patterning SU-8 2025 panels directly on top proved unsuccessful. By neglecting to first remove the 1827 resist, stresses were unintentionally incorporated into the panels, taking the form of rotating while folding in the hot water as shown in Figure 25.

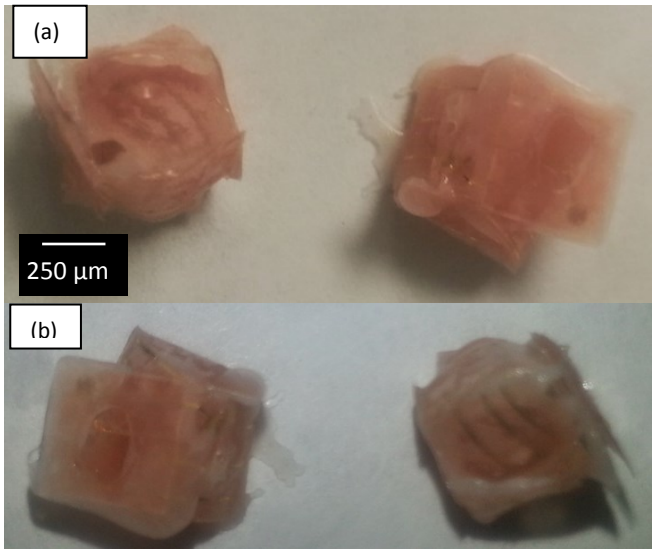

Figure 25: Improper Folding Due to Thin Film Stress. (a,b) Different views of thin film stress producing a rotation while folding. The pink color is a result of 1827 resist present on top of the clear SU-8.

By rinsing the wafer with acetone after electroplating this problem was completely eliminated, while leaving the wires completely intact.

Chapter 6: Self-Assembly and Applications

Self-assembly is the autonomous formation of disordered system into organized structure, and focuses on combining smaller discrete three-dimensional building blocks into a larger ordered structure [51][52][53]. It is one of the few bottom-up methods suited to give rise to functional structures on both the micro and macro scale [54]. This process occurs regularly in nature, such as how atoms or molecules arrange themselves into neatly ordered arrays or when amphiphilic surfactants self-assemble into micelles or liposomes when above a certain concentration in solution as driven by the hydrophobic effect and are held together by Van der Waals forces [36][55]. In addition to the hydrophobic effect there are many other 'smart' methods that can be harnessed to facilitate the discrete building blocks to self-assemble [56]. Biological examples include using ligands, peptides, protein and DNA due to the highly specific binding affinity to direct assembly [57][58].

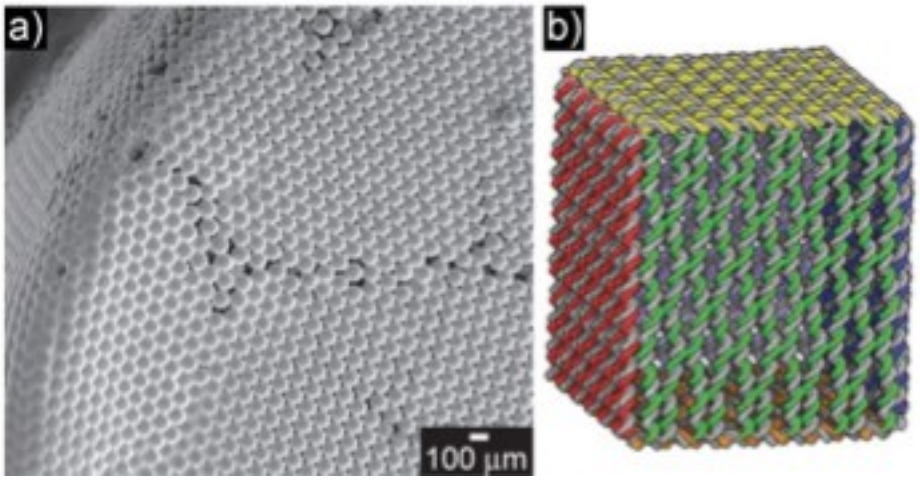

Figure 26: Structures Self-Assembled by Different Means. (a) SEM image of a 3D structure assembled with 80-micron colloidal crystals (b) Model of six DNA sheets arranged in a cubic structure with edge lengths around 40 nm. Reproduced from reference [36], © 2010, with permission from John Wiley and Sons.

Magnetism can also be used to self-assemble cells [59]. Block copolymers can also be made to self-assemble into a variety of shapes depending on the ratio of copolymers and the concentration in solution, as demonstrated by Eisenberg et al. [60]

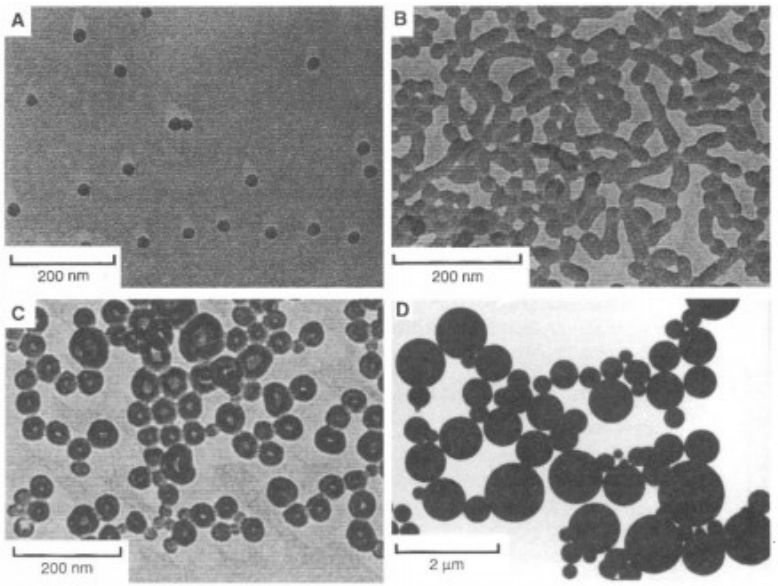

Figure 27: Multiple Morphologies of Self-Assembled Block Copolymer Aggregates. (a) Concentration near 10:1 styrene to acrylic acid yields spherical micelles (b) Decreasing the acrylic acid yields more rod shaped particles (c,d) further decreasing the styrene leads to poly-disperse vesicles. Reproduced from reference [60], reprinted with permission from AAAS.

Chapter 6.1: Pattern Directed Self-Assembly

A further advancement can be made if more complex restraints are imposed on the building blocks by selectively patterning the interconnections such that only a certain face may interact with another in a self-assembly method referred to as shape matching. This idea is most effective when the interacting structures are small, uniquely shaped to only fit together when properly aligned and adhere with the use of solder [47].

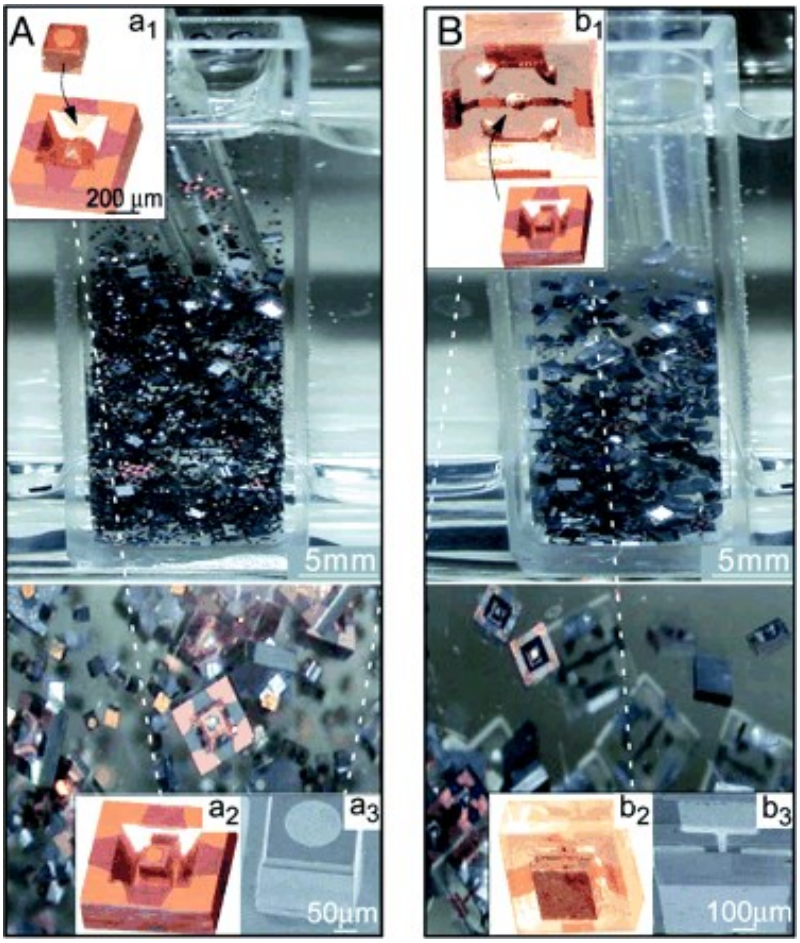

Figure 28: LED Chips Assembled via Pattern Recognition. Capital letters indicate photographs while lower case letter indicate micrographs. (a) Chip on carrier before assembly process (b) after assembly with correctly matched shapes. Reproduced from reference [47] © 2004, with permission from the National Academy of Sciences.

Inspired by the success of that approach, self-assembly was attempted with millimeter scale cubes resembling those previously self-folded. In lieu of using the self-folded polymer SU-8 cubes previously depicted, the first attempt at self-assembly focused on using commercially available wooden cubes with dimensions matching those of the 500 micron sized SU-8 cubes. The commercial availability of the wooden cubes permitted multiple, rapid and large-scale attempts at self-assembly. Without the substitution for the polymer SU-8 cubes, these attempts would otherwise not have been

feasible if the experiment were conducted only with the self-folded SU-8 polymer cubes due to the time constraints imposed by the multi-step fabrication process in combination with the relatively low yield.

Chapter 6.2: Building Blocks

To create building blocks suitable for shape matching self-assembly, a design initially featuring three concentric circles were patterned onto a pyralux sheet using photolithography. Pyralux is a thin, flexible material consisting of a polyimide polymer layer supporting a conductive copper clad laminate layer on top [61]. Each concentric circle design was affixed to one face of the cube with an epoxy resin to dictate the possible assembly interaction sites with other cubes. The composition of the pyralux and photolithography step allowed each of the concentric rings to contain a copper surface, while the spaces between them had the polymer exposed, as shown in Figure 29.

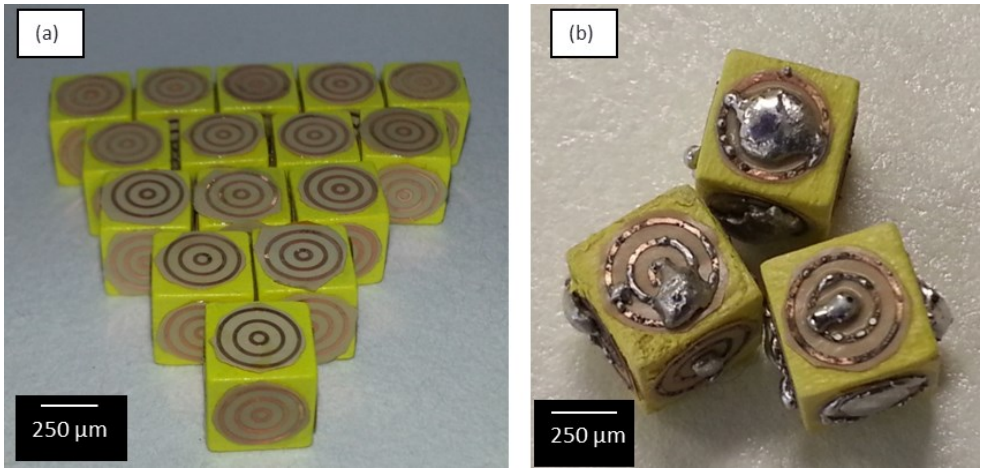

Figure 29: Building Blocks Representing Self-Folded Cubes for Self-Assembly. (a) Concentric circle pattern on wooden cubes (b) low melting point solder selectivity adhering to the copper rings.

The importance of the spacing lies in the ability to selectively deposit solder only on top of the concentric rings and not in the gaps between the rings. In the first method of applying solder via electroplating the exposed copper is essential, as the electroplating process requires the surface to conduct a charge to reduce the solder ions in solution and cause it to plate out at the copper acting as the cathode[62][63]. In the second method, called dip coating, a solid bock of low melting point solder, in this case a lead-tin solder with a melting point of 47° C, is heated to approximately 15 degrees above its melting point. The cubes can then be dipped into the molten solution at a 90-degree angle relative to the desired face to be coated. The affinity for the solder to selectively adhere to the copper layer can be explained by the favorable interfacial reactions occurring between the copper metal and tin and lead components in the solder [64]. With this pattern, the cubes can only assemble when the faces are perfectly aligned while discouraging assembly when the cubes are not at 90-degree angles relative to each other.

To facilitate self-assembly, the patterned cubes were put inside of a falcon tube filed with water and some liquid flux and placed in an incubated shaker set above the melting point of the solder overnight. The liquid flux is a solution of a highly concentrated acid, such as hydrochloric acid, with a low pH that dissolves any oxide layers formed by the interaction of the solder with the air after dip coating to increase the chance of a solid solder-to-solder connection to join the cubes together [65]. The water helps to reduce the gravitational forces preventing assembly [66].

Despite varying the range of temperature conditions from 50-100° C and the agitation speeds from 200-500 rpm, the cubes would not self-assemble. The solder was observed to melt so that assembly could occur, however the cube could not remain in contact with an

opposing solder face long enough for the solder to bond them. Further hampering the possibility to assemble was the fact that the wooden cubes were very buoyant in water resulting in them remaining near the top of the falcon tube. Combined with the small diameter of the falcon tube relative to the cube's dimensions, this effectively reduced the possible orientations that the cube could take and limited the interaction between faces capable of self-assembling.

Figure 30: Self-Assembly Issues. The buoyance of the wooden cubes combined with the small diameter of the falcon tube hampers self-assembly of the cubes. The red circle indicates solder that has melted off and settled on the bottom of the tube.

To rectify these issues, the material of the cube was changed along with the design of the copper pattern on the pyralux affixed to each face. The switch from wooden cubes to Poly (ethylene glycol)-diacrylate (PEG-DA) cubes was made to address the buoyancy problem, as the PEG-DA cubes would not accumulate at the top but distribute throughout the tube. The cubes were made using a reusable poly (dimethylsiloxane) (PDMS) molding technique that exactly replicated the size and shape of the wooden cubes with a high throughput rate to maintain the supply of cubes. First, the base and curing agents from the molding kit were mixed in a 10:1 (w/w) ratio and mixed thoroughly. The mixing created a large amount of bubbles, so the mixture was placed in a vacuum desiccator for an hour to remove them. After the desiccation, a thick but clear liquid remained. The wooden cubes to be used as the template were attached to the bottom of a petri dish using double-sided tape to prevent them from moving about when the liquid PDMA was poured into the petri dish. After pouring the PDMS into petri dish to completely cover the cubes, the solution was again placed in the desiccator for an hour to remove any bubbles. The elastomer was finally cured on a hotplate set to 50° C overnight. The solid PDMS can then be peeled off of the cubes to create a master mold. PEG-DA was chosen for the cube material because it can easily be poured into the mold and crosslinked under UV light to set the cube shape. When the PEG-DA was fully crosslinked the molded particles were easily pulled away from the master mold, yielding near identical replicas of the wooden cubes and preserving the master mold for future use.

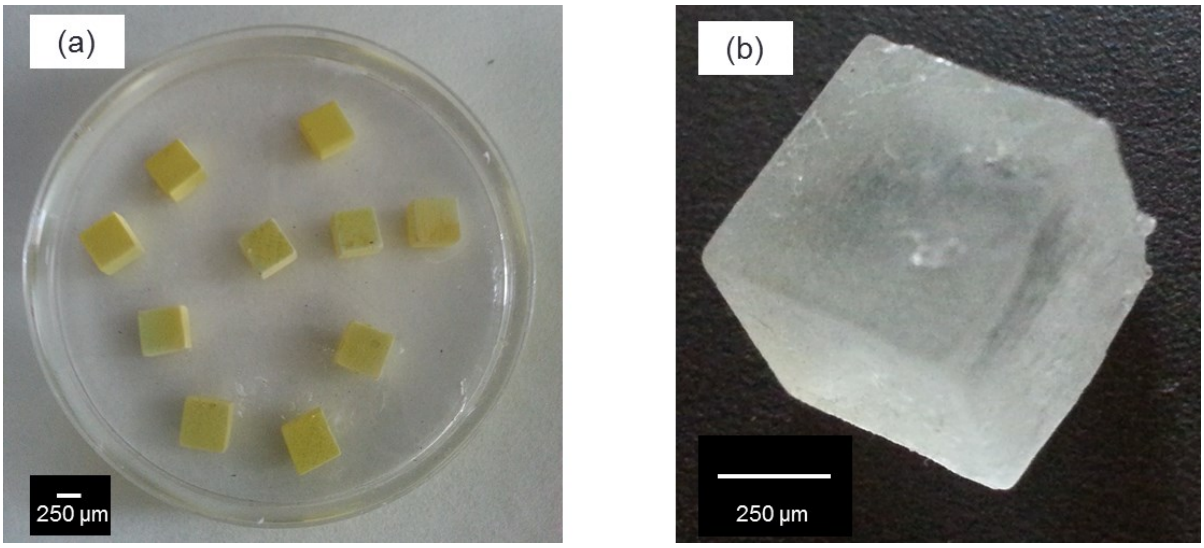

Figure 31: PDMS Molding of PEG-DA Cubes. (a) Wooden cubes taped to the bottom of the petri dish to produce a master mold with identical dimensions. (b) Molded PEG-DA polymer cube.

Studies indicated that for the best chance at self-assembly the volume of the solder on a face should be equal to the volume of the polyhedral to better support a strong adherence to each other [67]. With that in mind, the concentric circles were replaced with a single, solid circle encompassing most of the cube's face so that the volume of solder could more closely match that of the cube. This change had the adverse effect of allowing the solder to ball up and cover the entire area of the copper face, as there were no polymer gaps to restrict the adhesion of the solder, and led to uneven dip coating as shown in Figure 32.

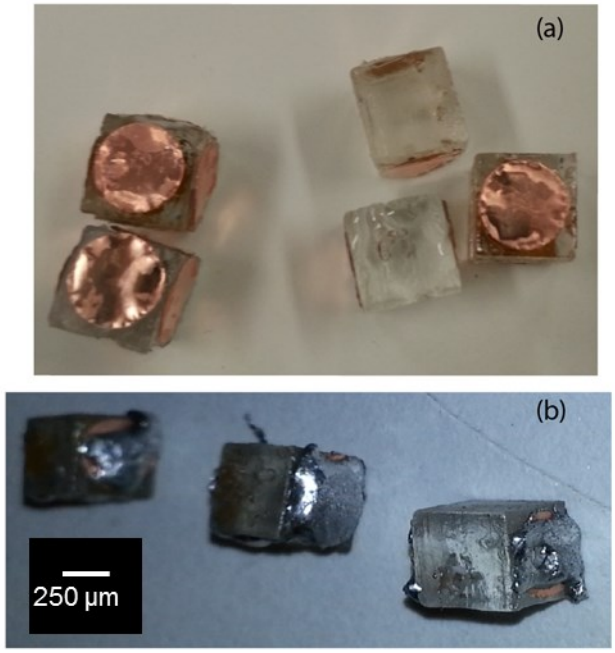

Figure 32: Improved Pattern for Shape Matching Self-Assembly. (a) PDMS cubes with the full circle pattern. (b) Uneven dip coating coverage and thickness on the full circle pyralux pattern.

Despite changing to a larger diameter vial to agitate the cubes and repeating the trials, a high degree of self-assembly was still not observed. During the shaking process the uneven thickness in the dip coated solder layer led to uneven solder melting. This drastically shortened the window of opportunity when two matching faces of adjacent cubes would collide with solder patterns sufficiently melted enough to join the cubes together. At temperatures far exceeding the melting point of the solder, or when the agitation was too aggressive, the solder tended to slide off of the copper pattern and pool at the bottom of the container. Efforts were made to change to a solder that could be electroplated onto the pyralux at a uniform thickness as determined by the electroplating time related by Faraday's law of electrolysis [68]. Unfortunately, the electroplated solder has a significantly high melting point of approximately 185° C. As such, water could no

longer be used for the liquid phase due to its 100-degree boiling point. N-Methyl-2-pyrrolidone (NMP) was substituted for water due to its slightly higher density and a boiling point in excess of 200° C. Experiments conducted with the NMP, liquid flux and electroplated solder faces revealed that temperatures sufficient to melt the solder would also degrade the epoxy resin used to bind the pyralux to the cubes, causing the pyralux to fall off of the cube and eliminate the possibility of self-assembly.

Successful assembly only occurred when the dip coated solder on the full circle pattern was affixed to the cubes, but placed in direct contact with each other to allow for an infinite window of opportunity for the solder on each cube's face to melt and join. It is important to note that when the cubes are in direct contact the assembly can take place in either liquid or aqueous environments.

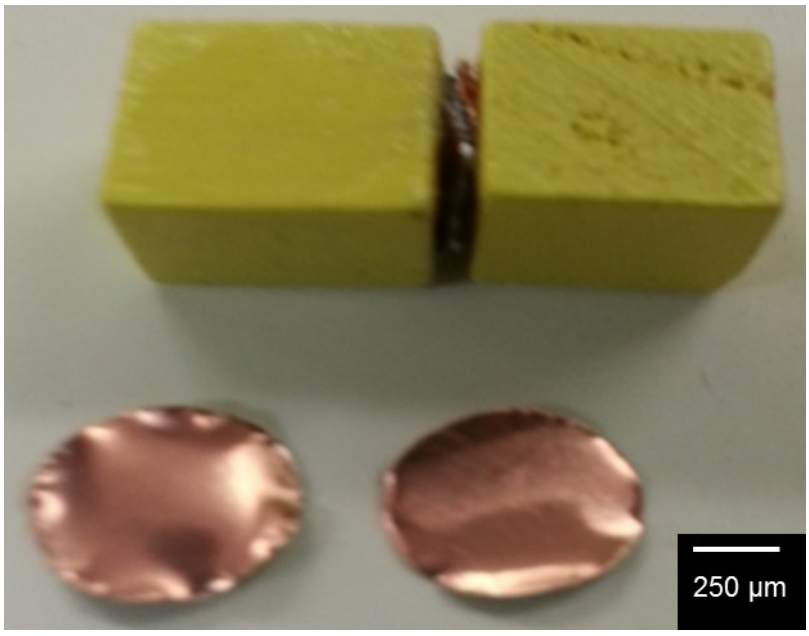

Figure 33: Linearly Assembled 500-micron Cubes. A pattern directed assembled cube connected by lead-tin low melting point solder.

Chapter 6.3: Discussion of Results

This chapter showed how surface patterns can be used to direct the assembly of small unit building blocks into larger ordered structures. Changes to the experimental setup resulted in better success rates for assembly. The switch from wood to polymer material for the cubes solved the buoyancy issues, while also allowing better comparison to the folded SU-8 cubes. Increasing the area of the circular surface pattern to better match the volume of the cube helped to afford more strength to the solder bonds forming between the cubes. Although only directed assembly was observed when the cubes were placed in contact with each other, the overall principles of self-assembly still apply. The next steps going forward involve augmenting this assembly process to increase the success rate of truly self-assembled structures.

Going forward, changes to address the solder, agitation and epoxy failures should be made to facilitate assembly. The agitation and temperature control issues could both be solved by using a rotary evaporator instead of placing the cubes into a tube and an incubated shaker. The rotary evaporator will provide a better quality of agitation over the incubated shaker, as the cubes will not be constrained by the tube. Instead the cubes can be swirled over a large volume with gently agitation that will not restrict the conformations of the cube to permit the faces of the cubes to come into contact with each other. Furthermore, rotary evaporators have good temperature control allowing the solder to melt enough to enable bonding, but not to melt off of the cubes and pool at the bottom of the container. The best hope at mitigating uneven solder thickness is to shy away from dip coating and replace it with electroplated solder. Electroplated solder offers uniform and precise thickness control, but the main drawback with the electroplated solder lies in

the high melting point that disrupts the epoxy bonding. Finding an epoxy that can stand up to temperatures in excess of 200° C would enable the use of the electroplated solder with a 185° C melting point and potentially solve the biggest obstacle to self-assembly. With these changes to address the issues, the self-assembly process would stand the best chance at success going forward.

Chapter 7: Conclusion and Future Outlook

This thesis has presented a couple different techniques designed to fabricate patterned structures in three dimensions on the micron to millimeter scale. Miniaturizing and finding a way to increase the density of integrated circuits without increasing the footprint has long been a major driving force in the computing industry. Various other methods have attempted to solve some of problems with traditional with computational devices, but do not truly take advantage of three-dimensional space and involve a great amount of manual fabrication.

The combination of self-folding, lithography and electroplating presented introduces new methods for fabricating polyhedral shaped three-dimensional integrated circuits. Separately, each of these three techniques are widely used and understood, however the combination of these three as presented in this thesis is a first step forward in the field toward three dimensional computing. It shows that the design and formation of self-folding of three dimensional computational devices is very realizable. It is one demonstration of a highly versatile process whose size scale, parallel processing capability and geometrical shapes can be altered to suit the designer's needs.

Although the concepts of self-folding and self-assembly are firmly established, the field of three dimensional computing is relatively new and continuously being explored. Further research into miniaturizing the size of the polyhedral, changing the shape of polyhedral and most importantly the self-assembly process will greatly advance this field to make it a commercially viable process to create more powerful computational devices while simultaneously decreasing their size.

Decreasing polyhedral size would allow for even higher density of electrical components to be fabricated on the same wafer. Additionally, decreasing the panel size would also decrease the weight of the panels which would help in the self-folding process. Development of a new polymeric hinge material that is photopatternable would completely eliminate the manual steps in the fabrication process while only adding another photolithography step. Another option for eliminating the manual PCL application step centers around modifying an inkjet printer to print the hinge material directly onto hinge gaps of the panels on the wafer. This would result in smooth and uniform amounts of hinge material perfectly aligned with the hinge gaps between the panels. Perfection of the solder based pattern dictated self-assembly process would enable autonomous mass scale assembly of these discrete circuits into a functional computer. Finally, a change in polyhedral from cube to a more complex shape such as an octahedron will still permit the units to assemble into an ordered structure, but with small gaps in the structure to allow air or another cooling fluid to be pumped through the assembly, potentially solving the important heating issue in electronics. This work hopes to pave the way for further research and advancement into the miniaturization and prevalence of three-dimensional computation technologies.

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Professional Experience

Researcher - Gracias Laboratory *September 2011 – August 2014*
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- Employed photolithographic techniques to design and fabricate three-dimensional metallic and polymeric circuits
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- Mentored and trained undergraduates in micro fabrication techniques

Education

The Johns Hopkins University - Baltimore, MD
M.S.E. Chemical and Biomolecular Engineering (August 2014)

- Thesis title: Assembly of 3D Microelectronic Blocks by Folding
- Course experience in solid state physics, nanomedicine and regenerative medicine.
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B.S. Chemical and Biomolecular Engineering (May 2013)

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Qualifications and Skills

- Excellent communication and team work skills
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